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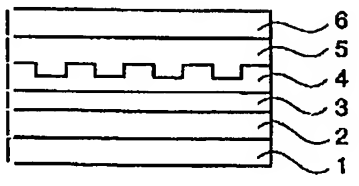
(54)【発明の名称】　強誘電体膜の製造方法および強誘電体素子

(57)【要約】
【課題】　高品質な強誘電体膜を製造する強誘電体膜の製造方法を提供する。
【解決手段】　基体表面に凹凸を形成する基体凹凸形成工程と、この基体表面に強誘電体を成膜する強誘電体成膜工程を備えることを特徴とする強誘電体膜の製造方法。



1：Si基板
2：シリコン酸化膜
3：Ti膜
4：下部電極Pt膜
5：強誘電体膜
6：上部電極Pt膜

【特許請求の範囲】
【請求項１】　基体表面に凹凸を形成する基体凹凸形成工程と、
この基体表面に強誘電体を成膜する強誘電体成膜工程を備えることを特徴とする強誘電体膜の製造方法。
【請求項２】　前記基体の凹部の幅が０．０５μｍ以上０．５μｍ以下であることを特徴とする請求項１記載の強誘電体膜の製造方法。
【請求項３】　表面に凹凸を有する基体と、
この基体表面に成膜された強誘電体膜を備えることを特徴とする強誘電体素子。
【請求項４】　表面に凹凸を有する基体と、
この基体表面に形成された強誘電体膜と、
この強誘電体膜上に形成されたゲート電極と、
このゲート電極を挟んで前記基体に形成された一対のソースドレイン領域を備えることを特徴とする強誘電体素子。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、半導体装置、特に強誘電体をゲート絶縁膜に使用する不揮発性メモリデバイスに関する。
【０００２】
【従来の技術】強誘電体を利用した記憶素子(FeRAM； FerroelectricRAM)は、不揮発性、高速性、ランダムアクセス性、書き換え回数耐性等の点で、DRAM、EEPROM(Electrically Erasable Programmable ROM)等の既存のメモリーに対して原理的に優位であり、活発な製品開発が進んでいる。ここで、強誘電体とは、ある特定の結晶方位に自発分極を有する誘電体をいい、その自発分極を外部電界で反転可能であることから、分極- 電界履歴特性を有する物質をいい、 PZT($Pb(Zr,Ti)O_3$)、SBT($SrBi_2Ta_2O_9$)などが挙げられる。
【０００３】FeRAM は、強誘電体という、従来の半導体素子では用いられてこなかった特殊な材料を用いるが故に、その信頼性において他の方式のメモリーに比較して未だ十分な水準に達していない。特に、強誘電体の膜質向上は、現在のFeRAM 開発技術における最も重要な項目のうちの一つである。
【０００４】強誘電体記憶素子の電気的な特性と強誘電体膜の構造的な特徴は、以下にその一例を示す通り、密接な関わりを有している。
(1) 強誘電体キャパシタ（MFM(Metal Ferroelectric Metal)キャパシタ）のリーク電流
MFM キャパシタのリーク電流はFeRAM の消費電流量を増大させるため、極力低減する必要がある。強誘電体の結晶粒子が大きいと、膜の表面モフォロジーが荒れ、上部電極材料が膜の谷間に入り込むことでキャパシタのリーク電流が増大することが知られている。また、結晶粒界にはコンダクティブな異相が形成されることが有り、これによってもリーク電流が増大する。例えば、 SBTにおいては、粒界にBiが高濃度に析出することが知られており、Biが金属のため、コンダクティブな性質を持つと考えられている。
【０００５】(2)残留分極量
FeRAM においては、MFM キャパシタをある極性に振ったときにキャパシタ外部に流れ出す分極反転電流によって記憶状態を読み出すため、強誘電体の残留分極量は高いことが望ましい。一般に、強誘電体粒子の粒径は大きい方が残留分極量も大きくなるといわれている。また、強誘電体膜が単一相で無く、強誘電相と常誘電相が混在していると残留分極量は低下する。また、粒界にトラップが発生することで、疲労耐性が劣化するとの報告もある。
【０００６】(3) 残留分極量の揺らぎ
上で述べたように強誘電体膜の粒径は残留分極確保の観点からは大きい方が望ましいが、粒径がキャパシタサイズと比較できるほどのサイズになると、キャパシタに含まれる強誘電体粒子の数の揺らぎや、個々の粒子の特性揺らぎが顕在化し、均一な特性を持つ記憶素子を実現するのが困難となる。
【０００７】以上の例で説明したとおり、FeRAM 高性能化における最大の課題は、高品質な強誘電体の成膜技術の開発である。具体的には、粒径、粒径の揺らぎ、粒密度、表面ラフネス、膜内応力といった良質化要因を制御することによって、高品質な強誘電体膜を製造することが可能となる。
【０００８】しかし、これらの良質化要因は、CVD(Chemical-Vapor-Deposition)法、スパッタ法、ゾルゲル法に代表されるような強誘電体の製造方法や、実験条件、実験装置、強誘電体を成膜する下地基板材料等、外部的な要因によって左右されやすく、統一的にこれらの要因を最適化することは非常に困難であった。このため、良質な強誘電体膜を得るためには、その都度最適な条件を見つけ出す必要があり、時間、物質的なロスが多かった。
【０００９】また、最適な条件といっても、例えば分極量の確保のためには粒径を大きく、低リーク電流の為には粒径を小さくというような互いに矛盾した要請もあり、本当の最適な条件というのは判断が難しいといえる。
【００１０】さらに、粒径の揺らぎのような問題は、従来の方法では制御することが困難で、特に素子の微細化が進み、強誘電体粒子と設計サイズが比較できるほどになってくると、この問題が顕在化することが予測される。
【００１１】上述のように、従来の強誘電体膜の製造方法では、粒径、粒密度、表面ラフネス、膜内応力といった強誘電体膜の良質化要因を効率よく制御し、粒径揺らぎのような本質的問題を解決して、強誘電体素子のための高品位強誘電体膜を提供することは困難になると考え

られる。

【0012】

【発明が解決しようとする課題】本発明は上述した問題点を考慮してなされたもので、その目的は、高品質な強誘電体膜を提供し、この高品質な強誘電体膜を用いた強誘電体素子を提供することである。

【0013】

【課題を解決するための手段】本願第1の発明は、基体表面に凹凸を形成する基体凹凸形成工程と、この基体表面に強誘電体を成膜する強誘電体成膜工程を備えることを特徴とする強誘電体膜の製造方法である。

【0014】本願第2の発明は、前記基体の凹部の幅が0．05μm以上0．5μm以下であることを特徴とする本願第1の発明に記載の強誘電体膜の製造方法である。本願第3の発明は、表面に凹凸を有する基体と、この基体表面に成膜された強誘電体膜を備えることを特徴とする強誘電体素子である。

【0015】本願第4の発明は、表面に凹凸を有する基体と、この基体表面に形成された強誘電体膜と、この強誘電体膜上に形成されたゲート電極と、このゲート電極を挟んで前記基体に形成された一対のソースドレイン領域を備えることを特徴とする強誘電体素子である。

【0016】本発明では、強誘電体を成膜するときの下地となる基体の形状のみの効果で強誘電体膜の良質化要因を制御することを特徴としている。凹凸を有する基体上に強誘電体を成膜することで、以下のような効果が得られる。

【0017】(1) 強誘電体結晶の核発生均一化

従来の方法では、強誘電体結晶の核発生はランダムに起こっていたが、下地基板に凹凸形状を持たせこれを核生成中心とすることで、均一な核発生を強制的に生じさせることが出来る。これにより、粒径が均一かつ粒界の少ない稠密な膜を形成できるうえ、粒径の増大、高配向性等の効果があるため、強誘電特性の向上が得られる。

【0018】(2) 強誘電体膜の歪み緩和

従来の方法では、平坦な下地基板上に強誘電体を成膜していたため、強誘電体膜は基板表面に平行な方向に互いに干渉しあい、歪みを含有する膜が形成されていた。

【0019】これに対し、本発明によれば、下地となる基体に凹凸形状を持たせることで、基体表面に平行方向の強誘電体膜の干渉の度合いが緩和され、歪みが少ない強誘電体膜を形成することができる。これにより、膜内歪みに起因した分極反転の阻害に代表されるような強誘電特性の劣化が低減されるばかりでなく、歪みの少ない環境で膜成長することにより粒界が少なく稠密な強誘電体膜が形成出来る。以上のことにより、強誘電体膜の性能が向上する。

【0020】

【発明の実施の形態】本発明は、凹凸を有する下地基体に対し強誘電体を成膜し、MFM キャパシタ、MFSFET(Metal-Ferroelectric-Semiconductor Field Effect Transistor) 等の強誘電体デバイス構造を形成することを特徴としている。下地基体の凹凸形状により、強誘電体膜は粒界が少なく、稠密で、表面モフォロジーが平坦な良質膜となる。以下、本発明の凹凸を有する下地基体上への強誘電体膜の製造方法と、この強誘電体膜を用いた強誘電体素子について、図面を参照しながら説明する。

【0021】図1は、第1の実施形態に係るFeRAM のMFM キャパシタ部分の断面図である。シリコン基板1上にシリコン酸化膜2 、その上に密着性を向上させるためのTi膜3、さらに下部電極Pt膜4が形成されている。下部電極Pt膜4には穴状の凸凹が形成されており、この上に強誘電体膜5、上部Pt電極6が形成され、MFM キャパシタを形成している。ここで、下地となる基体とは、下部電極Pt膜4だけであってもいいし、1から4までを含んでも良い。

【0022】なお、キャパシタ（電極で挟まれた誘電体）という意味では、4から6をMFMキャパシタという。次に、このMFM キャパシタの製造方法を図を用いて説明する。

【0023】まず、図2に示すようにシリコン基板1に対して、シリコン酸化膜2、Ti膜3、下部電極Pt膜4を堆積する。ここで、シリコン酸化膜はシリコン基板1と下部電極Pt膜4を電気的に絶縁するためのものであり、Ti膜3は下部電極Pt膜4とシリコン酸化膜2の密着性を向上させるためのものである。下部電極の材料はPtに限るわけではなく、Ir、IrO_2 、Ru、RuO_2 、$SrTiO_3$ 等、導電性を有する耐酸化性電極なら何でも良い。

【0024】次に、図3に示すように、下部電極Pt膜4に穴状の凹凸形状を加工する。下部電極Pt膜4上に円形の穴を開口するようなレジストパターンを光リソグラフィーあるいは電子ビーム露光により形成し、Arガスを用いたイオンミリングにより開口部のPtのみをエッチングする。この際、加工された下部電極Pt膜の形状的特徴は、一例として以下のようなものである。すなわち、初期の下部電極Pt膜4の膜厚は100nm、形成された凹部の深さは50nm、凹部の上面の形状は円形で、凹部の幅は0．5μmである。ここで、凹部の幅は、0．05μm以上0．5μm以下であることが好ましい。これは、0．5μmを超えると、前述した（1）強誘電体結晶の核発生均一化、及び（2）強誘電体膜の歪み緩和が困難になり、また、0．05μm未満では、強誘電体のサイズ効果によって強誘電性が消失してしまうからである。また、凹部の上面は矩形であってもよい。この時の凹部の幅とは、短い方の幅をいう。

【0025】次に、図4に示すように図3の基体上に強誘電体膜5を形成する。強誘電体膜は、ここでは一例としてSrBi2 Ta2 O9 (SBT)を、有機金属分解法（MOD(Metal Organic Decomposition)法）により形成した。MOD 法によるSBT の堆積条件は以下のようなものである。MOD

溶液をスピンコートにより回転速度１５００ｒｐｍ、回転時間２０秒の条件で基板上に塗布する。スピンコートの後、２００℃で５分試料を乾燥させ、溶液中の溶媒を揮発させる。スピンコートおよび乾燥工程を３回繰り返した後、８００℃の温度で３０分、大気圧酸素雰囲気中で熱処理し、SBT の結晶化を行なう。このようにして成膜されたSBT の膜厚は３００ｎｍ程度となる。このようにして形成したSBT 膜は、粒界が少なく、密度が高く、表面モフォロジーが平坦な良質膜となっている。さらにこの上に上部電極Pt膜６を形成し、図1 に示したようなMFM キャパシタが完成する。ここで、強誘電体の種類はSBT に限らず、 $Pb(Zr,Ti)O_3$ (PZT) 、$Bi_4Ti_3O_{12}$(BiTO) 等、どの材料でも構わないし、成膜方法はMOD 法以外の成膜方法でもよい。

【００２６】本実施形態に係る図１のMFM キャパシタは、凹凸形状を有さない平坦な下地電極上に形成した強誘電体膜による従来のMFM キャパシタと比較して、優れた電気的特性を示す。

【００２７】この理由は以下の通りである。図５に概念的に示したように、従来の方法で成膜した場合には多数の粒界を有し、粒径はばらつき、低密度で、表面モフォロジーが悪い。これに対して、本発明の方法によれば、粒の核発生制御や膜内歪みの低減といった効果によって、粒界が少なく、粒径のばらつきが少なく、膜密度が高く、表面モフォロジーの優れたものになるため、その電気的特性が改善する。

【００２８】さらに、図１から分かるように、このMFM キャパシタは２段階の膜厚を有するため、図６に概念的に示したように、書込電圧により２段階の分極量を記憶できる多値メモリへの応用が可能である。すなわち、図１において、下部電極Pt膜４から上部電極Pt膜６間に、強誘電体膜のうち膜厚が薄い部分のみが分極反転し、厚い部分は分極反転しないような電圧V_1 を印加すると、図６における残留分極P_1 を示すような書込みができる。さらに、強誘電体の厚い部分も薄い部分も共に分極反転するような電圧V_2 を書込み電圧として印加することにより、図６における残留分極P_2 を示すような書込みが出来る。書込み電圧によって２段階の分極を書込めるため、正負両方向で計4 つの記憶状態を有する多値メモリとしての動作が可能となる。本実施形態では一例として２段階の膜厚を持つ強誘電体を含有するようなMFM キャパシタで説明したが、膜厚をさらに段階的に変化させることでさらに多くの記憶状態を有する多値メモリを実現できる。もちろん、通常の動作電圧で強誘電体の最も厚い部分が分極反転するように強誘電体の膜厚を設定することで、通常の２値の記憶素子として利用する事も出来る。

【００２９】図７は、第２の実施形態に係る強誘電体ゲートFET （MFSFET(Metal Ferroelectric Semiconductor FET) ）の断面構造である。シリコン基板７上に、ソース/ ドレイン端に接した部分の薄いシリコン酸化膜１０、強誘電体膜１１からなるゲート絶縁膜、さらにゲート絶縁膜上のゲート電極１２で構成される島状領域が形成されている。前記島状領域の両側にはソース/ ドレイン領域９が形成されており、トレンチ８により素子分離がなされている。

【００３０】次に、このMFSFETの製造方法を図を用いて説明する。まず、図８に示すように、トレンチ８を有するシリコン基板７上に、シリコン酸化膜１０を堆積し、このシリコン酸化膜１０に対しゲート絶縁膜の一部となる強誘電体膜を形成するための穴を形成する。この際、シリコン酸化膜に開口する穴の寸法は、FET のチャネル部分が強誘電体に直に接する部分を決定するので、極力小さくするが、本実施形態では一例として０．２５μｍとする。また、シリコン酸化膜１０の膜厚は、本実施形態では一例として５ｎｍとする。

【００３１】次に、図９に示すように、強誘電体膜１１を、シリコン基板７とシリコン酸化膜１０で形成された凹凸を有する基体上に、例えばMOD 法により堆積する。このように凹部に埋め込まれるようにして堆積された強誘電体膜は、少なくともゲート絶縁膜となる凹部における部分では、図５に概念的に示したように、平坦な下地基板上に形成された強誘電体膜よりも良質な膜となる。

【００３２】さらに、図９の基板上にゲート電極を形成するための金属膜を堆積し、ゲート電極をパターニングするためのリソグラフィーを行い、金属膜、強誘電体膜、シリコン酸化膜をエッチングし、図１０のような構造を得る。引き続いてゲート電極をマスクとしてソース/ ドレイン領域形成のためのイオン注入を行い、注入された不純物を活性化するための熱処理を行なうことにより図７の様なMFSFETが完成する。

【００３３】本実施形態で形成されたMFSFETは、凹部に埋め込むようにして強誘電体を形成するために、従来の方法で形成された強誘電体膜によるMFSFETよりも良好な強誘電体特性を利用できる。さらに、このMFSFETでは、チャネルとゲート絶縁膜の界面において、ソース/ ドレイン端をはじめとして、ほとんどの界面領域がシリコン酸化膜で被覆されているために、拡散層リーク電流、界面準位が少なくMFSFETの基本性能が優れている。また、本実施形態のMFSFETでは、チャネル中央付近のみがMFS構造となっている。これにより、通常のMFSFETよりもゲート電極による強誘電体膜分極操作に対するドレイン電界の影響を受けにくく、記憶保持動作が安定しておこなわれるという特長を持っている。

【００３４】図１１は、第３の実施形態にかかるMFSFETの断面構造である。シリコン基板１３上に、T字型の強誘電体膜１８、その上にゲート電極１９が形成され、島状の領域が形成されている。島状領域はシリコン酸化膜１６および低誘電率膜１７（例えば、ＣＶＤによるシリコン酸化膜）で覆われている。島状領域の両端にはソー

ス/ ドレイン領域１５が形成され、LOCOS(Local Oxidationof Silicon) 酸化膜１４による素子分離がなされている。

【００３５】次に、このMFSFETの製造方法を図を用いて説明する。まず、図１２に示すように、LOCOS 酸化膜１４を有するシリコン基板１３上に堆積したpoly-Si 層２１をゲート電極のパターンに加工する。

【００３６】続いて、図１２の基板に対して拡散層を形成するためのイオン注入を行い、レジストを剥離し、不純物活性化の為の熱処理を行なう。さらに、シリコン酸化膜１６を全面に堆積し、平坦化を行なうことによって、図１３のような構造を得る。

【００３７】次に、図１４のように、図１３の基板のpoly-Si 層２１を例えばアルカリ溶液によりエッチングし、ゲート絶縁膜となる強誘電体を埋め込むための凹凸を有する基体（シリコン基板１３とシリコン酸化膜１６）を形成する。

【００３８】さらに、図１５のように、図１４の基板に対して強誘電体を例えばゾルゲル法等により成膜する。この時、強誘電体膜は、シリコン酸化膜１６から乖離し、シリコン基板１３に接した部分を支柱として膜全体が持ち上がるような形態を取る。一例として、凹部の幅が０．２５μm、凹部の深さが０．１μmの場合には、図１４のdは３０～４０nm程度となる。この持ち上げ高さd は、凹部の幅や深さを調整することで制御可能である。

【００３９】次に、図１６に示したように、図１５の強誘電体膜１８上に金属膜を堆積し、ゲート電極のレジストパターンを形成した後、金属膜、強誘電体膜１８の加工を行なうことにより、ゲート電極１９を含むT字型の島状領域を形成する。

【００４０】さらに、図１６の素子に対し低誘電率膜１７を堆積し、コンタクトホールを開口し、配線２０を作り込むことによって、図１１のMFSFETを得る事が出来る。本実施形態で形成されたMFSFETは、凹部に埋め込むようにして強誘電体を形成するために、従来の方法で形成された強誘電体膜によるMFSFETよりも良好な強誘電体特性を利用できる。さらに、本実施形態のMFSFETでは、強誘電体膜１８がシリコン酸化膜１６から乖離した構造を取っており、この空間を低誘電率膜１７で埋め込む構造を取っているために、ゲート電極１９とソース/ ドレイン領域１５の間に発生するゲート寄生容量を低減でき、MFSFETの基本的性能である動作速度が向上する。

【００４１】

【発明の効果】以上詳述したとおり、本発明の凹凸形状を有する下地基体を用いた強誘電体膜の製造方法により、良質な強誘電体膜を製造でき、さらにこの強誘電体膜を用いることによって、強誘電体素子の基本的性能を向上できる。

【図面の簡単な説明】

【図１】 本発明の第一の実施形態にかかるMFM キャパシタの断面図。

【図２】 本発明の第一の実施形態にかかるMFM キャパシタの製造工程を示す断面図。

【図３】 本発明の第一の実施形態にかかるMFM キャパシタの製造工程を示す断面図。

【図４】 本発明の第一の実施形態にかかるMFM キャパシタの製造工程を示す断面図。

【図５】 本発明における、基板の凹凸形状による強誘電体膜質向上の原理を示す模式図。

【図６】 本発明の第一の実施形態にかかるMFM キャパシタの、多値メモリとしての応用例を示すP-V 曲線の概念図。

【図７】 本発明の第二の実施形態にかかるMFSFETの断面図。

【図８】 本発明の第二の実施形態にかかるMFSFETの製造工程を示す断面図。

【図９】 本発明の第二の実施形態にかかるMFSFETの製造工程を示す断面図。

【図１０】 本発明の第二の実施形態にかかるMFSFETの製造工程を示す断面図。

【図１１】 本発明の第三の実施形態にかかるMFSFETの断面図。

【図１２】 本発明の第三の実施形態にかかるMFSFETの製造工程を示す断面図。

【図１３】 本発明の第三の実施形態にかかるMFSFETの製造工程を示す断面図。

【図１４】 本発明の第三の実施形態にかかるMFSFETの製造工程を示す断面図。

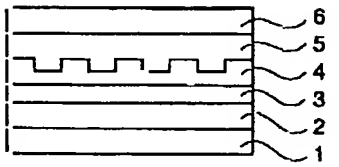
【図１５】 本発明の第三の実施形態にかかるMFSFETの製造工程を示す断面図。

【図１６】 本発明の第三の実施形態にかかるMFSFETの製造工程を示す断面図。

【符号の説明】

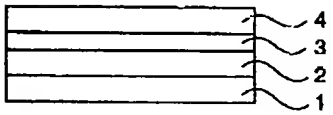
１，７，１３　Ｓｉ基板
２，１０　シリコン酸化膜
３　Ｔｉ膜
４　下部電極Ｐｔ膜
５，１１，１８　強誘電体膜
６　上部電極Ｐｔ膜
８　トレンチ
９，１５　ソース/ ドレイン領域
１２　ゲート電極
１４　LOCOS 酸化膜
１６　シリコン酸化膜
１７　低誘電率膜
１９　ゲート電極
２０　配線
２１　poly-Si 層
２２　レジスト

【図1】



1：Si基板
2：シリコン酸化膜
3：Ti膜
4：下部電極Pt膜
5：強誘電体膜
6：上部電極Pt膜

【図2】



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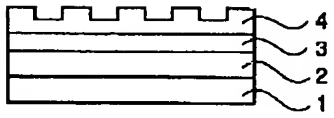

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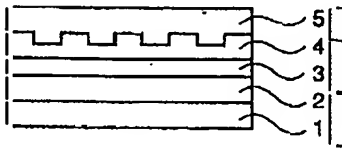

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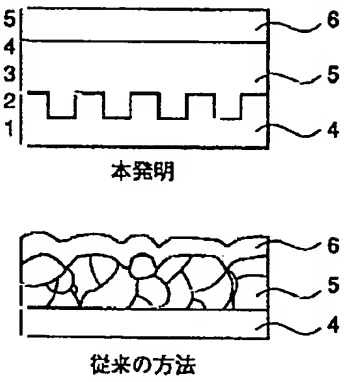

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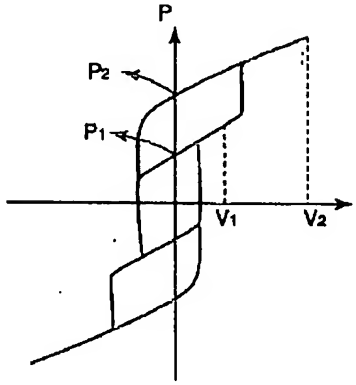

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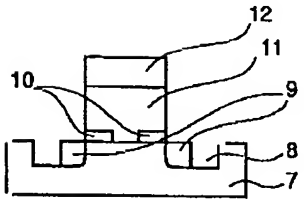
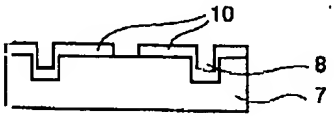


7：Si基板
8：トレンチ
9：ソース／ドレイン領域
10：シリコン酸化膜
11：強誘電体膜
12：ゲート電極

【図8】



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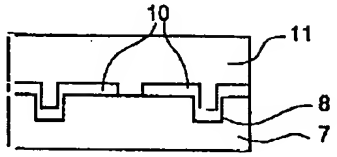

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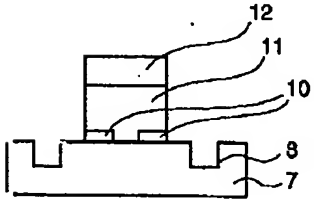

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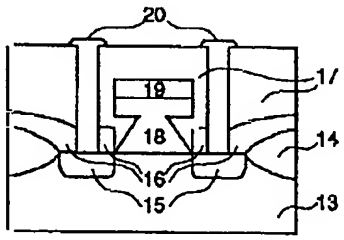
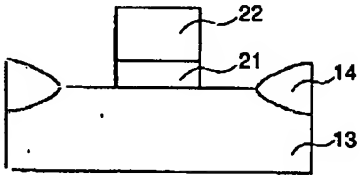


13：Si基板
14：LOCOS酸化膜
15：ソース／ドレイン領域
16：シリコン酸化膜
17：低誘電率膜
18：強誘電体膜
19：ゲート電極
20：配線
21：poly-Si層
22：レジスト

【図12】



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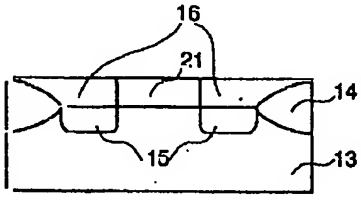

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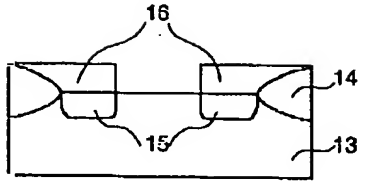

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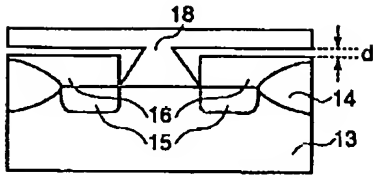

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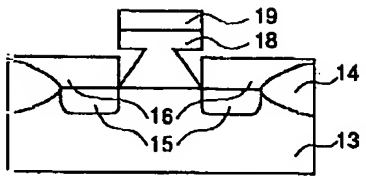

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CLAIMS

[Claim(s)]
[Claim 1] The manufacture approach of the ferroelectric film characterized by having the base irregularity formation process which forms irregularity in a base front face, and the ferroelectric membrane formation process which forms a ferroelectric on this base front face.
[Claim 2] The manufacture approach of the ferroelectric film according to claim 1 that width of face of the crevice of said base is characterized by 0.05-micrometer or more being 0.5 micrometers or less.
[Claim 3] The ferroelectric component characterized by having the base which has irregularity on a front face, and the ferroelectric film formed by this base front face.
[Claim 4] The ferroelectric component characterized by having the source drain field of the pair formed in the front face at said base on both sides of the base which has irregularity, the ferroelectric film formed in this base front face, the gate electrode formed on this ferroelectric film, and this gate electrode.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the non-volatile memory device which uses a semiconductor device, especially a ferroelectric for gate dielectric film.
[0002]
[Description of the Prior Art] The storage elements (FeRAM; FerroelectricRAM) using a ferroelectric are points, such as a non-volatile, rapidity, random access nature, and count resistance of rewriting, to the existing memory, such as DRAM and EEPROM (Electrically Erasable Programmable ROM), it is dominance theoretically and the active product development is progressing. polarization [since a ferroelectric can say the dielectric which has spontaneous polarization to a certain specific crystal orientation here and the spontaneous polarization can be reversed by external electric field] - the matter which has an electric-field hysteresis property is said -- PZT (Pb(Zr, Ti) O 3) and SBT (SrBi2 Ta 2O9) etc. -- it is mentioned.
[0003] FeRAM In a conventional semiconductor device called a ferroelectric, although the special ingredient which was not used is used therefore, in the dependability, still sufficient level is not reached as compared with the memory of other methods. Especially the improvement in membraneous of a ferroelectric is current FeRAM. It is one of the most important items in a development technique.
[0004] The electric property of a ferroelectric storage element and the structural description of the ferroelectric film have close relation as they show the example below.
(1) Leakage current MFM of a ferroelectric capacitor (MFM (Metal Ferroelectric Metal) capacitor) The leakage current of a capacitor is FeRAM. In order to increase the amount of consumed electric currents, it is necessary to decrease as much as possible. If the crystal grain child of a ferroelectric is large, it is known that the leakage current of a capacitor will increase because a dry area and an up electrode material enter [membranous surface morphology] a membranous valley. Moreover, a KONDAKUTIBU unusual appearance is sometimes formed in a grain boundary, and leakage current increases also by this. For example, in SBT, it is known that Bi deposits in a grain boundary at high concentration, and since Bi is a metal, it is thought that it has a KONDAKUTIBU property.

[0005] (2) The amount FeRAM of remanences It sets and is MFM. When a capacitor is shaken at a certain polarity, in order to read a storage condition according to the polarization reversal current which flows into the capacitor exterior, the high thing of the amount of remanences of a ferroelectric is desirable. Generally, the one where the particle size of a ferroelectric particle is larger is said to become large also for the amount of remanences. Moreover, there is no ferroelectric film at a single phase, and if the ferroelectric phase and the paraelectric phase are intermingled, the amount of remanences will fall. Moreover, there is also a report that fatigue resistance deteriorates because a trap occurs in a grain boundary.
[0006] (3) It is on fluctuation of the amount of remanences, as stated, from a viewpoint of remanence reservation, the larger one of the particle size of the ferroelectric film is desirable but, if particle size becomes size to the extent that it can compare with capacitor size, fluctuation of the number of ferroelectric particles contained in a capacitor and the property fluctuation of each particle will actualize, and it will become difficult to realize a storage element with a uniform property.
[0007] It is FeRAM as the above example explained. The biggest technical problem in high-performance-izing is development of the membrane formation technique of a quality ferroelectric. Specifically, it becomes possible by controlling good-ized factors, such as fluctuation of particle size and particle size, a grain consistency, surface roughness, and film internal stress, to manufacture the quality ferroelectric film.
[0008] however, these good-ized factors -- CVD (Chemical-Vapor-Deposition) -- it was very difficult for external factors, such as the manufacture approach of a ferroelectric which is represented by law, a spatter, and the sol gel process, and a substrate substrate ingredient which forms experiment conditions, an experimental device, and a ferroelectric, to be easy to be influenced, and to optimize these factors systematically. For this reason, in order to obtain the good ferroelectric film, the optimal conditions needed to be found out each time and there were many time amount and material losses.
[0009] Moreover, even if it calls it the optimal conditions, for reservation of the amount of polarization, it is large in particle size, and for low leakage current, there is also a request which says that particle size is small and which was mutually contradictory, and it can be said that decision is difficult for the optimal true conditions, for example.
[0010] Furthermore, if it becomes so that a problem [particle size] like fluctuation is difficult to control by the conventional approach, especially detailed-ization of a component progresses and a ferroelectric particle can be compared with design size, it will be predicted that this problem actualizes.
[0011] As mentioned above, by the manufacture approach of the conventional ferroelectric film, the good-ized factor of ferroelectric film, such as particle size, a grain consistency, surface roughness, and film internal stress, is controlled efficiently, an essential problem like particle-size fluctuation is solved, and it is thought that it becomes difficult to offer the high definition ferroelectric film for a ferroelectric component.

[0012]
[Problem(s) to be Solved by the Invention] This invention is having been made in consideration of the trouble mentioned above, and that purpose's offering the quality ferroelectric film, and offering the ferroelectric component using this quality ferroelectric film.
[0013]
[Means for Solving the Problem] This application the 1st invention is the manufacture approach of the ferroelectric film characterized by having the base irregularity formation process which forms irregularity in a base front face, and the ferroelectric membrane formation process which forms a ferroelectric on this base front face.
[0014] This application the 2nd invention is the manufacture approach of the ferroelectric film given in this application the 1st invention to which the width of face of the crevice of said base considers that it is [0.05 micrometer or more] 0.5 micrometers or less as the description. This application the 3rd invention is a ferroelectric component characterized by having the base which has irregularity on a front face, and the ferroelectric film formed by this base front face.
[0015] This application the 4th invention is a ferroelectric component characterized by having the source drain field of the pair formed in the front face at said base on both sides of the base which has irregularity, the ferroelectric film formed in this base front face, the gate electrode formed on this ferroelectric film, and this gate electrode.
[0016] In this invention, it is characterized by controlling the good-ized factor of the ferroelectric film by effectiveness of only the configuration of the base used as the substrate when forming a ferroelectric. The following effectiveness is acquired by forming a ferroelectric on the base which has irregularity.
[0017] (1) By the approach of the karyogenesis equalization former of a ferroelectric crystal, although the karyogenesis of a ferroelectric crystal had happened at random, it is giving the shape of toothing to a substrate substrate and setting this as a nucleation core, and can produce uniform karyogenesis compulsorily. In particle size's being able to form homogeneity and the dense film with few grain boundaries by this, since there is effectiveness, such as increase of particle size and the tropism of your kind consideration, the improvement in strong dielectric characteristics is obtained.
[0018] (2) By the approach of the strain relaxation former of the ferroelectric film, since the ferroelectric was formed on the flat substrate substrate, it interfered in the ferroelectric film mutually, it suited in the direction parallel to a substrate front face, and the film containing distortion was formed.
[0019] On the other hand, according to this invention, by giving the shape of toothing to the base used as a substrate, the degree of interference of the parallel ferroelectric film on a base front face is eased, and distortion can form little ferroelectric film. Degradation of strong dielectric characteristics which is represented by inhibition of the polarization reversal resulting from the distortion in the film by this is not only reduced, but it can form the ferroelectric film with them by carrying out film growth in an environment with little distortion. [there are few grain boundaries and dense] The engine performance of the ferroelectric film

improves by the above thing.
[0020]
[Embodiment of the Invention] the substrate base with which this invention has irregularity -- receiving -- a ferroelectric -- forming membranes -- MFM A capacitor and MFSFET (Metal-Ferroelectric-Semiconductor Field Effect Transistor) etc. -- it is characterized by forming ferroelectric device structure. According to the shape of toothing of a substrate base, the ferroelectric film has few grain boundaries, and is dense, and it becomes the good-quality film with flat surface morphology. Hereafter, the ferroelectric component using this ferroelectric film is explained to be the manufacture approach of the ferroelectric film to the substrate base top which has the irregularity of this invention, referring to a drawing.
[0021] Drawing 1 is FeRAM concerning the 1st operation gestalt. MFM It is the sectional view of a capacitor part. The lower electrode Pt film 4 is formed in the Ti film 3 for raising adhesion silicon oxide 2 and on it on a silicon substrate 1, and a pan. Hole-like unevenness is formed in the lower electrode Pt film 4, the ferroelectric film 5 and the up Pt electrode 6 are formed on this, and it is MFM. The capacitor is formed. Here, the base used as a substrate may be only the lower electrode Pt film 4, and even 1-4 may also be included.
[0022] In addition, in the semantics of a capacitor (dielectric inserted with the electrode), 4-6 are called MFM capacitor. Next, this MFM The manufacture approach of a capacitor is explained using drawing.
[0023] First, as shown in drawing 2 , silicon oxide 2, the Ti film 3, and the lower electrode Pt film 4 are deposited to a silicon substrate 1. Silicon oxide is here for insulating electrically a silicon substrate 1 and the lower electrode Pt film 4, and the Ti film 3 is for raising the adhesion of the lower electrode Pt film 4 and silicon oxide 2. the ingredient of a lower electrode is restricted to Pt -- ********** -- IrIrO 2 Ru and RuO 2 SrTiO 3 etc. -- if it is the oxidation-resistant electrode which has conductivity, it is good anything.
[0024] Next, as shown in drawing 3 , the shape of hole-like toothing is processed into the lower electrode Pt film 4. A resist pattern which carries out opening of the circular hole on the lower electrode Pt film 4 is formed by optical lithography or electron beam exposure, and only Pt of opening is etched by the ion milling using Ar gas. Under the present circumstances, the geometrical description of the processed lower electrode Pt film is as follows as an example. That is, the configuration of the top face of 50nm and a crevice of the depth of the crevice in which 100nm of thickness of the early lower electrode Pt film 4 was formed is circular, and the width of face of a crevice is 0.5 micrometers. Here, as for the width of face of a crevice, it is desirable that it is [0.05 micrometer or more] 0.5 micrometers or less. This is because karyogenesis equalization of (1) ferroelectric crystal mentioned above and the strain relaxation of (2) ferroelectric film will become difficult and a ferroelectricity will disappear according to the size effect of a ferroelectric in less than 0.05 micrometers, if it exceeds 0.5 micrometers. Moreover, the top face of a crevice may be a rectangle. The width of face of the crevice at this time means the width of face of the shorter one.
[0025] Next, as shown in drawing 4 , the ferroelectric film 5 is formed on the base

of drawing 3 . The ferroelectric film formed SrBi2 Ta 2O9 (SBT) as an example here by the organic metal part solution method (MOD (Metal Organic Decomposition) law). MOD SBT by law Deposition conditions are as follows. MOD A solution is applied on a substrate with a spin coat on rotational-speed 1500rpm and the conditions for turnover time 20 seconds. A sample is dried at 200 degrees C behind a spin coat for 5 minutes, and the solvent in a solution is volatilized. After repeating a spin coat and a desiccation process 3 times, it heat-treats in an atmospheric pressure oxygen ambient atmosphere at the temperature of 800 degrees C for 30 minutes, and it is SBT. It crystallizes. Thus, formed SBT Thickness is set to about 300nm. Thus, formed SBT The film has few grain boundaries, and its consistency is high and it is the good-quality film with flat surface morphology. Furthermore, the up electrode Pt film 6 is formed on this, and it is drawing 1. MFM as shown A capacitor is completed. here -- the class of ferroelectric -- SBT not only -- Pb(Zr, Ti) O 3 (PZT) and Bi4 Ti 3O12 (BiTO) etc. -- any ingredient is sufficient -- carrying out -- the membrane formation approach -- MOD law -- the membrane formation approach of an except may be used.

[0026] MFM of drawing 1 concerning this operation gestalt A capacitor is the conventional MFM by the ferroelectric film formed on the flat substrate electrode which does not have the shape of toothing. Outstanding electrical characteristics are shown as compared with a capacitor.

[0027] This reason is as follows. As notionally shown in drawing 5 , when membranes are formed by the conventional approach, it has many grain boundaries, and particle size is dispersion and a low consistency and its surface morphology is bad. On the other hand, according to the approach of this invention, according to effectiveness, such as karyogenesis control of a grain and reduction of the distortion in the film, there are few grain boundaries, there is little dispersion in particle size, a film consistency is high, and since it becomes what was excellent in surface morphology, the electrical characteristics improve.

[0028] Furthermore, it is this MFM so that drawing 1 may show. Since a capacitor has two steps of thickness, as notionally shown in drawing 6 , the application to the multiple-value memory which can memorize two steps of the amounts of polarization with a write-in electrical potential difference is possible for it. That is, it is the electrical potential difference V1 in which only a part with thin thickness carries out polarization reversal among ferroelectric film between the up electrode Pt film 6 from the lower electrode Pt film 4, and a thick part does not carry out polarization reversal in drawing 1 R> 1. Remanence P1 in drawing 6 if it impresses Writing as shown is made. Furthermore, electrical potential difference V2 in which both the thick part of a ferroelectric and a thin part carry out polarization reversal Remanence [in / by impressing as a write-in electrical potential difference / drawing 6] P2 Writing as shown is made. Since two steps of polarization can be written in with a write-in electrical potential difference, it is a total of 4 in positive/negative both directions. The actuation as multiple-value memory which has the storage condition of ** is attained. MFM which contains the ferroelectric which has two steps of thickness as an example with this operation gestalt Although the capacitor explained, the multiple-value memory which has the storage condition of further many [change / thickness / still more gradually] is

realizable. Of course, it can also use as a storage element binary [usual] by setting up the thickness of a ferroelectric so that the thickest part of a ferroelectric may carry out polarization reversal with the usual operating voltage.
[0029] Drawing 7 is the cross-section structure of the ferroelectric gate FET concerning the 2nd operation gestalt (MFSFET (Metal Ferroelectric Semiconductor FET)). On a silicon substrate 7, it is source/. The gate dielectric film which consists of silicon oxide 10 with the thin part which touched the drain edge, and ferroelectric film 11, and the island-like field which consists of gate electrodes 12 on gate dielectric film further are formed. In the both sides of said island-like field, it is source/. The drain field 9 is formed and isolation is made with the trench 8.
[0030] Next, the manufacture approach of this MFSFET is explained using drawing. First, as shown in drawing 8 , silicon oxide 10 is deposited on the silicon substrate 7 which has a trench 8, and the hole for forming the ferroelectric film which turns into some gate dielectric film to this silicon oxide 10 is formed. Under the present circumstances, the dimension of the hole which carries out opening to silicon oxide is FET. Although it is made small as much as possible since the part to which a channel part touches a ferroelectric soon is determined, with this operation gestalt, it may be 0.25 micrometers as an example. Moreover, the thickness of silicon oxide 10 may be 5nm as an example with this operation gestalt.
[0031] Next, it is MOD on the base which has the irregularity formed by the silicon substrate 7 and silicon oxide 10 in the ferroelectric film 11 as shown in drawing 9 . It deposits by law. Thus, it is embedded in a crevice, and in the part in the crevice which serves as gate dielectric film at least, the ferroelectric film made and deposited turns into film better than the ferroelectric film formed on the flat substrate substrate, as notionally shown in drawing 5 .
[0032] Furthermore, the metal membrane for forming a gate electrode on the substrate of drawing 9 is deposited, lithography for carrying out patterning of the gate electrode is performed, a metal membrane, the ferroelectric film, and silicon oxide are etched, and structure like drawing 10 is acquired. It is source/, using a gate electrode as a mask succeedingly. MFSFET like drawing 7 is completed by performing heat treatment for performing the ion implantation for drain field formation, and activating the poured-in impurity.
[0033] MFSFET formed with this operation gestalt can use a ferroelectric property better than MFSFET by the ferroelectric film formed by the conventional approach, in order to form a ferroelectric, as it embeds in a crevice. Furthermore, in this MFSFET, it sets to the interface of a channel and gate dielectric film, and is source/. Since almost all interface fields including a drain edge are covered with silicon oxide, there are little diffusion layer leakage current and interface state density, and the fundamentality ability of MFSFET is excellent. Moreover, at MFSFET of this operation gestalt, near a channel center is MFS. It has structure. It has the features of being [of drain electric field] hard to be influenced to the ferroelectric film polarization actuation by the gate electrode by the usual MFSFET, and being carried out by stabilizing storage maintenance actuation by this.
[0034] Drawing 11 is the cross-section structure of MFSFET concerning the 3rd operation gestalt. On a silicon substrate 13, the ferroelectric film 18 of a T

character mold is formed, the gate electrode 19 is formed on it, and the island-like field is formed. The island-like field is covered by silicon oxide 16 and the low dielectric constant film 17 (for example, silicon oxide by CVD). In the both ends of an island-like field, it is source/. The drain field 15 is formed and it is LOCOS (Local Oxidationof Silicon). The isolation by the oxide film 14 is made.

[0035] Next, the manufacture approach of this MFSFET is explained using drawing. First, it is LOCOS as shown in drawing 12 . poly-Si deposited on the silicon substrate 13 which has an oxide film 14 A layer 21 is processed into the pattern of a gate electrode.

[0036] Then, the ion implantation for forming a diffusion layer to the substrate of drawing 12 is performed, a resist is exfoliated, and heat treatment for impurity activation is performed. Furthermore, silicon oxide 16 is deposited on the whole surface, and structure like drawing 13 is acquired by performing flattening.

[0037] Next, it is poly-Si of the substrate of drawing 13 like drawing 14 . A layer 21 is etched for example, with an alkali solution, and the base (a silicon substrate 13 and silicon oxide 16) which has the irregularity for embedding the ferroelectric used as gate dielectric film is formed.

[0038] Furthermore, a ferroelectric is formed with a sol gel process etc. to the substrate of drawing 14 like drawing 15 . At this time, the ferroelectric film deviates from silicon oxide 16, and takes a gestalt in which the whole film is lifted by using as a stanchion the part which touched the silicon substrate 13. As an example, as for d of drawing 14 , the depth of 0.25 micrometers and a crevice is set to about 30-40nm by it, when the width of face of a crevice is 0.1 micrometers. this -- raising -- height d It is controllable by adjusting the width of face and the depth of a crevice.

[0039] Next, as shown in drawing 16 , after depositing a metal membrane on the ferroelectric film 18 of drawing 15 and forming the resist pattern of a gate electrode, the island-like field of the T character mold containing the gate electrode 19 is formed by performing processing of a metal membrane and the ferroelectric film 18.

[0040] Furthermore, MFSFET of drawing 11 can be obtained by depositing the low dielectric constant film 17 to the component of drawing 16 , carrying out opening of the contact hole, and making wiring 20. MFSFET formed with this operation gestalt can use a ferroelectric property better than MFSFET by the ferroelectric film formed by the conventional approach, in order to form a ferroelectric, as it embeds in a crevice. Furthermore, since the structure in which the ferroelectric film 18 deviated from silicon oxide 16 is taken and the structure which embeds this space by the low dielectric constant film 17 is taken in MFSFET of this operation gestalt, they are the gate electrode 19 and source/. The gate parasitic capacitance generated between the drain fields 15 can be reduced, and the working speed which is the fundamental engine performance of MFSFET improves.

[0041]

[Effect of the Invention] The fundamental engine performance of a ferroelectric component can be improved by being able to manufacture the good ferroelectric film and using this ferroelectric film further by the manufacture approach of the ferroelectric film using the substrate base which has the shape of toothing of this

invention, as explained in full detail above.

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the non-volatile memory device which uses a semiconductor device, especially a ferroelectric for gate dielectric film.

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PRIOR ART

[Description of the Prior Art] The storage elements (FeRAM; FerroelectricRAM) using a ferroelectric are points, such as a non-volatile, rapidity, random access nature, and count resistance of rewriting, to the existing memory, such as DRAM and EEPROM (Electrically Erasable Programmable ROM), it is dominance theoretically and the active product development is progressing. polarization [since a ferroelectric can say the dielectric which has spontaneous polarization to a certain specific crystal orientation here and the spontaneous polarization can be reversed by external electric field] - the matter which has an electric-field hysteresis property is said -- PZT (Pb(Zr, Ti) O 3) and SBT (SrBi2 Ta 2O9) etc. -- it is mentioned.
[0003] FeRAM In a conventional semiconductor device called a ferroelectric, although the special ingredient which was not used is used therefore, in the dependability, still sufficient level is not reached as compared with the memory of other methods. Especially the improvement in membraneous of a ferroelectric is current FeRAM. It is one of the most important items in a development technique.
[0004] The electric property of a ferroelectric storage element and the structural description of the ferroelectric film have close relation as they show the example below.
(1) Leakage current MFM of a ferroelectric capacitor (MFM (Metal Ferroelectric Metal) capacitor) The leakage current of a capacitor is FeRAM. In order to increase the amount of consumed electric currents, it is necessary to decrease as much as possible. If the crystal grain child of a ferroelectric is large, it is known that the leakage current of a capacitor will increase because a dry area and an up electrode material enter [membranous surface morphology] a membranous valley. Moreover, a KONDAKUTIBU unusual appearance is sometimes formed in a grain boundary, and leakage current increases also by this. For example, in SBT, it is known that Bi deposits in a grain boundary at high concentration, and since Bi is a metal, it is thought that it has a KONDAKUTIBU property.
[0005] (2) The amount FeRAM of remanences It sets and is MFM. When a capacitor is shaken at a certain polarity, in order to read a storage condition according to the polarization reversal current which flows into the capacitor exterior, the high thing of the amount of remanences of a ferroelectric is desirable. Generally, the one where the particle size of a ferroelectric particle is larger is said to become large also for the amount of remanences. Moreover, there is no

ferroelectric film at a single phase, and if the ferroelectric phase and the paraelectric phase are intermingled, the amount of remanences will fall. Moreover, there is also a report that fatigue resistance deteriorates because a trap occurs in a grain boundary.

[0006] (3) It is on fluctuation of the amount of remanences, as stated, from a viewpoint of remanence reservation, the larger one of the particle size of the ferroelectric film is desirable but, if particle size becomes size to the extent that it can compare with capacitor size, fluctuation of the number of ferroelectric particles contained in a capacitor and the property fluctuation of each particle will actualize, and it will become difficult to realize a storage element with a uniform property.

[0007] It is FeRAM as the above example explained. The biggest technical problem in high-performance-izing is development of the membrane formation technique of a quality ferroelectric. Specifically, it becomes possible by controlling good-ized factors, such as fluctuation of particle size and particle size, a grain consistency, surface roughness, and film internal stress, to manufacture the quality ferroelectric film.

[0008] however, these good-ized factors -- CVD (Chemical-Vapor-Deposition) -- it was very difficult for external factors, such as the manufacture approach of a ferroelectric which is represented by law, a spatter, and the sol gel process, and a substrate substrate ingredient which forms experiment conditions, an experimental device, and a ferroelectric, to be easy to be influenced, and to optimize these factors systematically. For this reason, in order to obtain the good ferroelectric film, the optimal conditions needed to be found out each time and there were many time amount and material losses.

[0009] Moreover, even if it calls it the optimal conditions, for reservation of the amount of polarization, it is large in particle size, and for low leakage current, there is also a request which says that particle size is small and which was mutually contradictory, and it can be said that decision is difficult for the optimal true conditions, for example.

[0010] Furthermore, if it becomes so that a problem [particle size] like fluctuation is difficult to control by the conventional approach, especially detailed-ization of a component progresses and a ferroelectric particle can be compared with design size, it will be predicted that this problem actualizes.

[0011] As mentioned above, by the manufacture approach of the conventional ferroelectric film, the good-ized factor of ferroelectric film, such as particle size, a grain consistency, surface roughness, and film internal stress, is controlled efficiently, an essential problem like particle-size fluctuation is solved, and it is thought that it becomes difficult to offer the high definition ferroelectric film for a ferroelectric component.

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EFFECT OF THE INVENTION

[Effect of the Invention] The fundamental engine performance of a ferroelectric component can be improved by being able to manufacture the good ferroelectric film and using this ferroelectric film further by the manufacture approach of the ferroelectric film using the substrate base which has the shape of toothing of this invention, as explained in full detail above.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] This invention is having been made in consideration of the trouble mentioned above, and that purpose's offering the quality ferroelectric film, and offering the ferroelectric component using this quality ferroelectric film.

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MEANS

[Means for Solving the Problem] This application the 1st invention is the manufacture approach of the ferroelectric film characterized by having the base irregularity formation process which forms irregularity in a base front face, and the ferroelectric membrane formation process which forms a ferroelectric on this base front face.
[0014] This application the 2nd invention is the manufacture approach of the ferroelectric film given in this application the 1st invention to which the width of face of the crevice of said base considers that it is [0.05 micrometer or more] 0.5 micrometers or less as the description. This application the 3rd invention is a ferroelectric component characterized by having the base which has irregularity on a front face, and the ferroelectric film formed by this base front face.
[0015] This application the 4th invention is a ferroelectric component characterized by having the source drain field of the pair formed in the front face at said base on both sides of the base which has irregularity, the ferroelectric film formed in this base front face, the gate electrode formed on this ferroelectric film, and this gate electrode.
[0016] In this invention, it is characterized by controlling the good-ized factor of the ferroelectric film by effectiveness of only the configuration of the base used as the substrate when forming a ferroelectric. The following effectiveness is acquired by forming a ferroelectric on the base which has irregularity.
[0017] (1) By the approach of the karyogenesis equalization former of a ferroelectric crystal, although the karyogenesis of a ferroelectric crystal had happened at random, it is giving the shape of toothing to a substrate substrate and setting this as a nucleation core, and can produce uniform karyogenesis compulsorily. In particle size's being able to form homogeneity and the dense film with few grain boundaries by this, since there is effectiveness, such as increase of particle size and the tropism of your kind consideration, the improvement in strong dielectric characteristics is obtained.
[0018] (2) By the approach of the strain relaxation former of the ferroelectric film, since the ferroelectric was formed on the flat substrate substrate, it interfered in the ferroelectric film mutually, it suited in the direction parallel to a substrate front face, and the film containing distortion was formed.
[0019] On the other hand, according to this invention, by giving the shape of toothing to the base used as a substrate, the degree of interference of the parallel

ferroelectric film on a base front face is eased, and distortion can form little ferroelectric film. Degradation of strong dielectric characteristics which is represented by inhibition of the polarization reversal resulting from the distortion in the film by this is not only reduced, but it can form the ferroelectric film with them by carrying out film growth in an environment with little distortion. [there are few grain boundaries and dense] The engine performance of the ferroelectric film improves by the above thing.

[0020]

[Embodiment of the Invention] the substrate base with which this invention has irregularity -- receiving -- a ferroelectric -- forming membranes -- MFM A capacitor and MFSFET (Metal-Ferroelectric-Semiconductor Field Effect Transistor) etc. -- it is characterized by forming ferroelectric device structure. According to the shape of toothing of a substrate base, the ferroelectric film has few grain boundaries, and is dense, and it becomes the good-quality film with flat surface morphology. Hereafter, the ferroelectric component using this ferroelectric film is explained to be the manufacture approach of the ferroelectric film to the substrate base top which has the irregularity of this invention, referring to a drawing.

[0021] Drawing 1 is FeRAM concerning the 1st operation gestalt. MFM It is the sectional view of a capacitor part. The lower electrode Pt film 4 is formed in the Ti film 3 for raising adhesion silicon oxide 2 and on it on a silicon substrate 1, and a pan. Hole-like unevenness is formed in the lower electrode Pt film 4, the ferroelectric film 5 and the up Pt electrode 6 are formed on this, and it is MFM. The capacitor is formed. Here, the base used as a substrate may be only the lower electrode Pt film 4, and even 1-4 may also be included.

[0022] In addition, in the semantics of a capacitor (dielectric inserted with the electrode), 4-6 are called MFM capacitor. Next, this MFM The manufacture approach of a capacitor is explained using drawing.

[0023] First, as shown in drawing 2 , silicon oxide 2, the Ti film 3, and the lower electrode Pt film 4 are deposited to a silicon substrate 1. Silicon oxide is here for insulating electrically a silicon substrate 1 and the lower electrode Pt film 4, and the Ti film 3 is for raising the adhesion of the lower electrode Pt film 4 and silicon oxide 2. the ingredient of a lower electrode is restricted to Pt -- ********** -- IrIrO 2 Ru and RuO 2 SrTiO 3 etc. -- if it is the oxidation-resistant electrode which has conductivity, it is good anything.

[0024] Next, as shown in drawing 3 , the shape of hole-like toothing is processed into the lower electrode Pt film 4. A resist pattern which carries out opening of the circular hole on the lower electrode Pt film 4 is formed by optical lithography or electron beam exposure, and only Pt of opening is etched by the ion milling using Ar gas. Under the present circumstances, the geometrical description of the processed lower electrode Pt film is as follows as an example. That is, the configuration of the top face of 50nm and a crevice of the depth of the crevice in which 100nm of thickness of the early lower electrode Pt film 4 was formed is circular, and the width of face of a crevice is 0.5 micrometers. Here, as for the width of face of a crevice, it is desirable that it is [0.05 micrometer or more] 0.5 micrometers or less. This is because karyogenesis equalization of (1) ferroelectric

crystal mentioned above and the strain relaxation of (2) ferroelectric film will become difficult and a ferroelectricity will disappear according to the size effect of a ferroelectric in less than 0.05 micrometers, if it exceeds 0.5 micrometers. Moreover, the top face of a crevice may be a rectangle. The width of face of the crevice at this time means the width of face of the shorter one.

[0025] Next, as shown in drawing 4 , the ferroelectric film 5 is formed on the base of drawing 3 . The ferroelectric film formed SrBi2 Ta 2O9 (SBT) as an example here by the organic metal part solution method (MOD (Metal Organic Decomposition) law). MOD SBT by law Deposition conditions are as follows. MOD A solution is applied on a substrate with a spin coat on rotational-speed 1500rpm and the conditions for turnover time 20 seconds. A sample is dried at 200 degrees C behind a spin coat for 5 minutes, and the solvent in a solution is volatilized. After repeating a spin coat and a desiccation process 3 times, it heat-treats in an atmospheric pressure oxygen ambient atmosphere at the temperature of 800 degrees C for 30 minutes, and it is SBT. It crystallizes. Thus, formed SBT Thickness is set to about 300nm. Thus, formed SBT The film has few grain boundaries, and its consistency is high and it is the good-quality film with flat surface morphology. Furthermore, the up electrode Pt film 6 is formed on this, and it is drawing 1. MFM as shown A capacitor is completed. here -- the class of ferroelectric -- SBT not only -- Pb(Zr, Ti) O 3 (PZT) and Bi4 Ti 3O12 (BiTO) etc. -- any ingredient is sufficient -- carrying out -- the membrane formation approach -- MOD law -- the membrane formation approach of an except may be used.

[0026] MFM of drawing 1 concerning this operation gestalt A capacitor is the conventional MFM by the ferroelectric film formed on the flat substrate electrode which does not have the shape of toothing. Outstanding electrical characteristics are shown as compared with a capacitor.

[0027] This reason is as follows. As notionally shown in drawing 5 , when membranes are formed by the conventional approach, it has many grain boundaries, and particle size is dispersion and a low consistency and its surface morphology is bad. On the other hand, according to the approach of this invention, according to effectiveness, such as karyogenesis control of a grain and reduction of the distortion in the film, there are few grain boundaries, there is little dispersion in particle size, a film consistency is high, and since it becomes what was excellent in surface morphology, the electrical characteristics improve.

[0028] Furthermore, it is this MFM so that drawing 1 may show. Since a capacitor has two steps of thickness, as notionally shown in drawing 6 , the application to the multiple-value memory which can memorize two steps of the amounts of polarization with a write-in electrical potential difference is possible for it. That is, it is the electrical potential difference V1 in which only a part with thin thickness carries out polarization reversal among ferroelectric film between the up electrode Pt film 6 from the lower electrode Pt film 4, and a thick part does not carry out polarization reversal in drawing 1 R> 1. Remanence P1 in drawing 6 if it impresses Writing as shown is made. Furthermore, electrical potential difference V2 in which both the thick part of a ferroelectric and a thin part carry out polarization reversal Remanence [in / by impressing as a write-in electrical potential difference / drawing 6] P2 Writing as shown is made. Since two steps of polarization can be

written in with a write-in electrical potential difference, it is a total of 4 in positive/negative both directions. The actuation as multiple-value memory which has the storage condition of ** is attained. MFM which contains the ferroelectric which has two steps of thickness as an example with this operation gestalt Although the capacitor explained, the multiple-value memory which has the storage condition of further many [change / thickness / still more gradually] is realizable. Of course, it can also use as a storage element binary [usual] by setting up the thickness of a ferroelectric so that the thickest part of a ferroelectric may carry out polarization reversal with the usual operating voltage.

[0029] Drawing 7 is the cross-section structure of the ferroelectric gate FET concerning the 2nd operation gestalt (MFSFET (Metal Ferroelectric Semiconductor FET)). On a silicon substrate 7, it is source/. The gate dielectric film which consists of silicon oxide 10 with the thin part which touched the drain edge, and ferroelectric film 11, and the island-like field which consists of gate electrodes 12 on gate dielectric film further are formed. In the both sides of said island-like field, it is source/. The drain field 9 is formed and isolation is made with the trench 8.

[0030] Next, the manufacture approach of this MFSFET is explained using drawing. First, as shown in drawing 8 , silicon oxide 10 is deposited on the silicon substrate 7 which has a trench 8, and the hole for forming the ferroelectric film which turns into some gate dielectric film to this silicon oxide 10 is formed. Under the present circumstances, the dimension of the hole which carries out opening to silicon oxide is FET. Although it is made small as much as possible since the part to which a channel part touches a ferroelectric soon is determined, with this operation gestalt, it may be 0.25 micrometers as an example. Moreover, the thickness of silicon oxide 10 may be 5nm as an example with this operation gestalt.

[0031] Next, it is MOD on the base which has the irregularity formed by the silicon substrate 7 and silicon oxide 10 in the ferroelectric film 11 as shown in drawing 9 . It deposits by law. Thus, it is embedded in a crevice, and in the part in the crevice which serves as gate dielectric film at least, the ferroelectric film made and deposited turns into film better than the ferroelectric film formed on the flat substrate substrate, as notionally shown in drawing 5 .

[0032] Furthermore, the metal membrane for forming a gate electrode on the substrate of drawing 9 is deposited, lithography for carrying out patterning of the gate electrode is performed, a metal membrane, the ferroelectric film, and silicon oxide are etched, and structure like drawing 10 is acquired. It is source/, using a gate electrode as a mask succeedingly. MFSFET like drawing 7 is completed by performing heat treatment for performing the ion implantation for drain field formation, and activating the poured-in impurity.

[0033] MFSFET formed with this operation gestalt can use a ferroelectric property better than MFSFET by the ferroelectric film formed by the conventional approach, in order to form a ferroelectric, as it embeds in a crevice. Furthermore, in this MFSFET, it sets to the interface of a channel and gate dielectric film, and is source/. Since almost all interface fields including a drain edge are covered with silicon oxide, there are little diffusion layer leakage current and interface state density, and the fundamentality ability of MFSFET is excellent. Moreover, at MFSFET of this operation gestalt, near a channel center is MFS. It has structure.

It has the features of being [of drain electric field] hard to be influenced to the ferroelectric film polarization actuation by the gate electrode by the usual MFSFET, and being carried out by stabilizing storage maintenance actuation by this.

[0034] Drawing 11 is the cross-section structure of MFSFET concerning the 3rd operation gestalt. On a silicon substrate 13, the ferroelectric film 18 of a T character mold is formed, the gate electrode 19 is formed on it, and the island-like field is formed. The island-like field is covered by silicon oxide 16 and the low dielectric constant film 17 (for example, silicon oxide by CVD). In the both ends of an island-like field, it is source/. The drain field 15 is formed and it is LOCOS (Local Oxidationof Silicon). The isolation by the oxide film 14 is made.

[0035] Next, the manufacture approach of this MFSFET is explained using drawing. First, it is LOCOS as shown in drawing 12 . poly-Si deposited on the silicon substrate 13 which has an oxide film 14 A layer 21 is processed into the pattern of a gate electrode.

[0036] Then, the ion implantation for forming a diffusion layer to the substrate of drawing 12 is performed, a resist is exfoliated, and heat treatment for impurity activation is performed. Furthermore, silicon oxide 16 is deposited on the whole surface, and structure like drawing 13 is acquired by performing flattening.

[0037] Next, it is poly-Si of the substrate of drawing 13 like drawing 14 . A layer 21 is etched for example, with an alkali solution, and the base (a silicon substrate 13 and silicon oxide 16) which has the irregularity for embedding the ferroelectric used as gate dielectric film is formed.

[0038] Furthermore, a ferroelectric is formed with a sol gel process etc. to the substrate of drawing 14 like drawing 15 . At this time, the ferroelectric film deviates from silicon oxide 16, and takes a gestalt in which the whole film is lifted by using as a stanchion the part which touched the silicon substrate 13. As an example, as for d of drawing 14 , the depth of 0.25 micrometers and a crevice is set to about 30-40nm by it, when the width of face of a crevice is 0.1 micrometers. this -- raising -- height d It is controllable by adjusting the width of face and the depth of a crevice.

[0039] Next, as shown in drawing 16 , after depositing a metal membrane on the ferroelectric film 18 of drawing 15 and forming the resist pattern of a gate electrode, the island-like field of the T character mold containing the gate electrode 19 is formed by performing processing of a metal membrane and the ferroelectric film 18.

[0040] Furthermore, MFSFET of drawing 11 can be obtained by depositing the low dielectric constant film 17 to the component of drawing 16 , carrying out opening of the contact hole, and making wiring 20. MFSFET formed with this operation gestalt can use a ferroelectric property better than MFSFET by the ferroelectric film formed by the conventional approach, in order to form a ferroelectric, as it embeds in a crevice. Furthermore, since the structure in which the ferroelectric film 18 deviated from silicon oxide 16 is taken and the structure which embeds this space by the low dielectric constant film 17 is taken in MFSFET of this operation gestalt, they are the gate electrode 19 and source/. The gate parasitic capacitance generated between the drain fields 15 can be reduced, and the

working speed which is the fundamental engine performance of MFSFET improves.

[Translation done.]

* NOTICES *

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] MFM concerning the first operation gestalt of this invention Sectional view of a capacitor.
[Drawing 2] MFM concerning the first operation gestalt of this invention Sectional view showing the production process of a capacitor.
[Drawing 3] MFM concerning the first operation gestalt of this invention Sectional view showing the production process of a capacitor.
[Drawing 4] MFM concerning the first operation gestalt of this invention Sectional view showing the production process of a capacitor.
[Drawing 5] The mimetic diagram showing the principle of the improvement in ferroelectric membraneous by the shape of toothing of a substrate in this invention.
[Drawing 6] MFM concerning the first operation gestalt of this invention P-V which shows the application as multiple-value memory of a capacitor Curved conceptual diagram.
[Drawing 7] The sectional view of MFSFET concerning the second operation gestalt of this invention.
[Drawing 8] The sectional view showing the production process of MFSFET concerning the second operation gestalt of this invention.
[Drawing 9] The sectional view showing the production process of MFSFET concerning the second operation gestalt of this invention.
[Drawing 10] The sectional view showing the production process of MFSFET concerning the second operation gestalt of this invention.
[Drawing 11] The sectional view of MFSFET concerning the third operation gestalt of this invention.
[Drawing 12] The sectional view showing the production process of MFSFET concerning the third operation gestalt of this invention.
[Drawing 13] The sectional view showing the production process of MFSFET concerning the third operation gestalt of this invention.
[Drawing 14] The sectional view showing the production process of MFSFET concerning the third operation gestalt of this invention.
[Drawing 15] The sectional view showing the production process of MFSFET concerning the third operation gestalt of this invention.
[Drawing 16] The sectional view showing the production process of MFSFET

concerning the third operation gestalt of this invention.

[Description of Notations]

1, 7, 13 Si substrate
2 Ten Silicon oxide
3 Ti Film
4 Lower Electrode Pt Film
5, 11, 18 Ferroelectric film
6 Up Electrode Pt Film
8 Trench
9 15 Source/Drain field
12 Gate Electrode
14 LOCOS Oxide Film
16 Silicon Oxide
17 Low Dielectric Constant Film
19 Gate Electrode
20 Wiring
21 Poly-Si Layer
22 Resist

[Translation done.]

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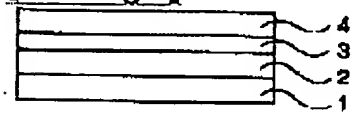
DRAWINGS

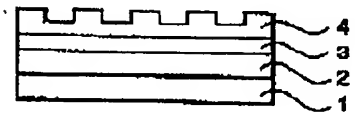
[Drawing 1]

1：Si基板
2：シリコン酸化膜
3：Ti膜
4：下部電極Pt膜
5：強誘電体膜
6：上部電極Pt膜

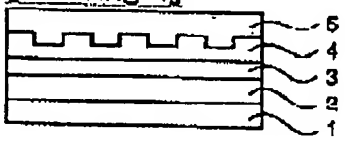
[Drawing 2]



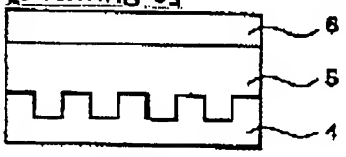
[Drawing 3]



[Drawing 4]



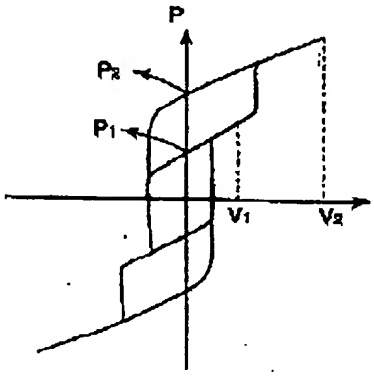
[Drawing 5]



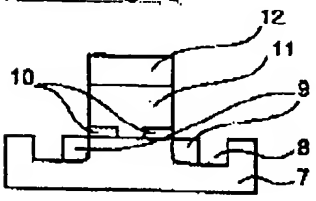
本発明

従来の方法

[Drawing 6]

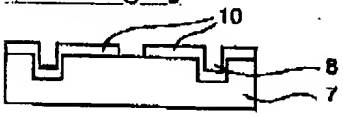


[Drawing 7]

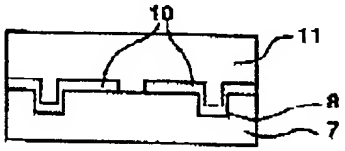


7：Si基板
8：トレンチ
9：ソース／ドレイン領域
10：シリコン酸化膜
11：強誘電体膜
12：ゲート電極

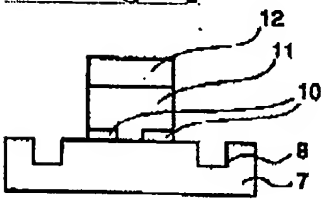
[Drawing 8]



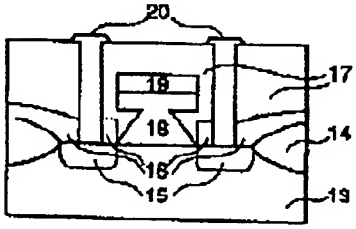
[Drawing 9]



[Drawing 10]

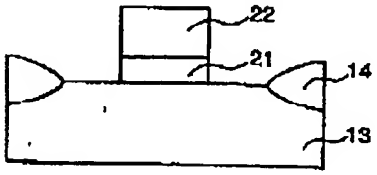


[Drawing 11]

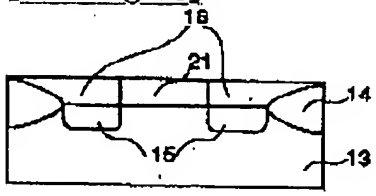


13：Si基板
14：LOCOS酸化膜
15：ソース／ドレイン領域
16：シリコン酸化膜
17：低誘電率膜
18：強誘電体膜
19：ゲート電極
20：配線
21：poly-Si層
22：レジスト

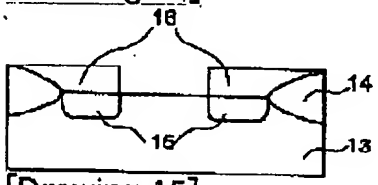
[Drawing 12]



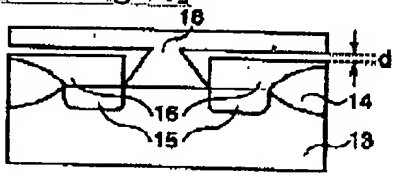
[Drawing 13]



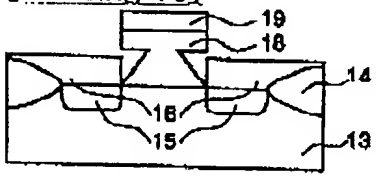
[Drawing 14]



[Drawing 15]



[Drawing 16]



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